Title: CONTROLLER DRIVER AND DISPLAY APPARATUS USING THE SAME
Inventor(s): Hirobumi FURIHATA et al.
DOCKET NO.: 074273-0242

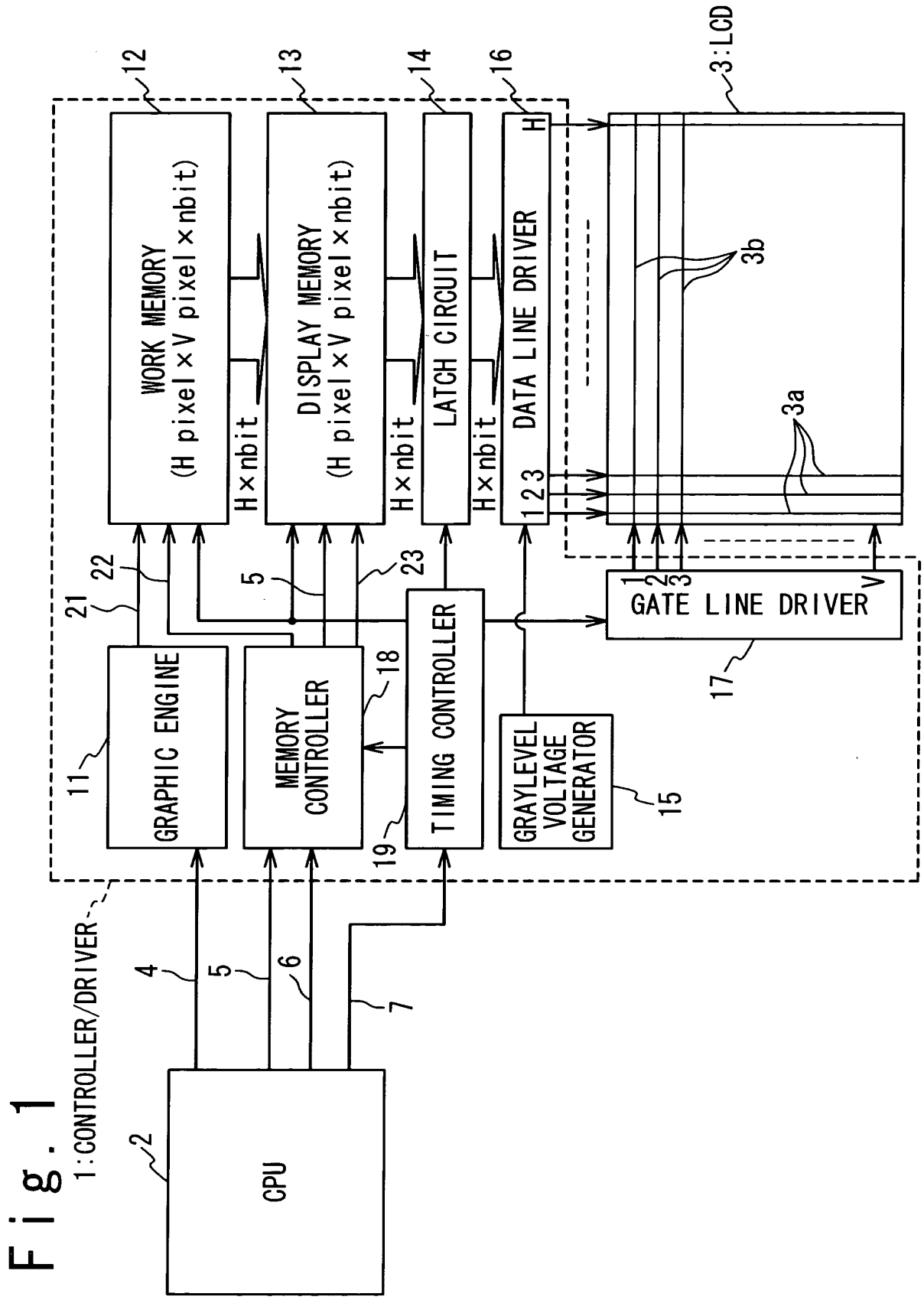


Fig. 1

Fig. 2

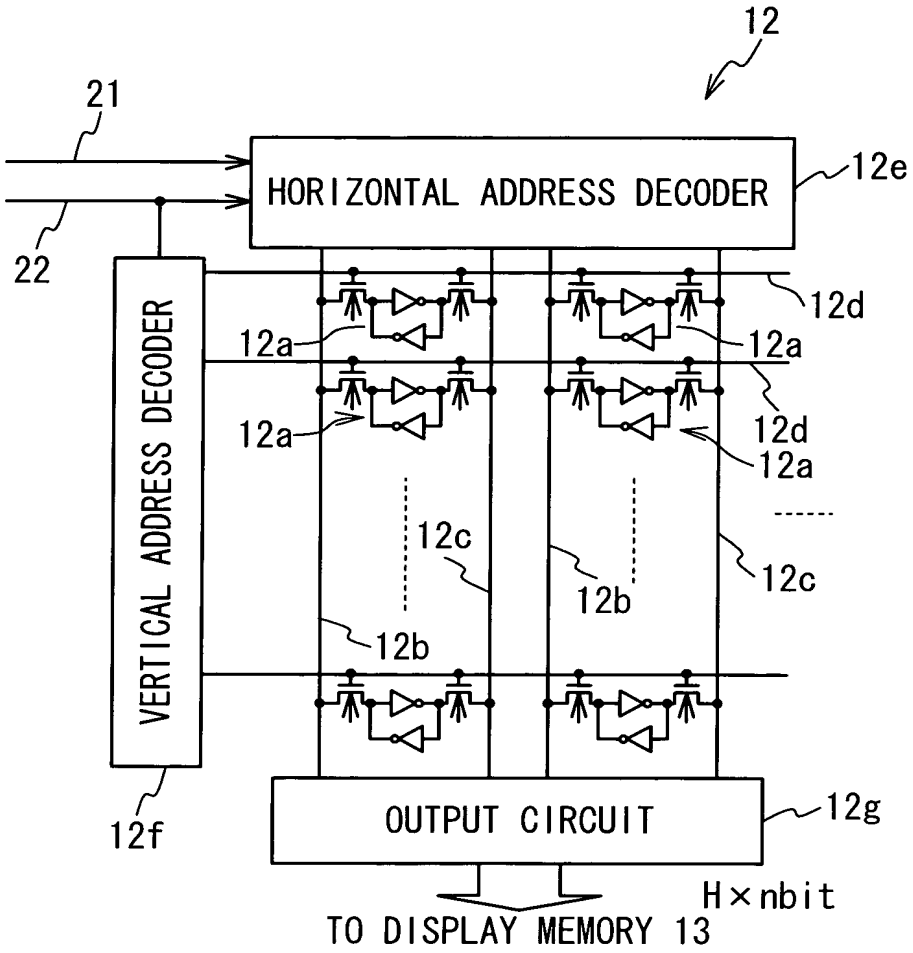

12
21
22
HORIZONTAL ADDRESS DECODER
12e
VERTICAL ADDRESS DECODER
12f
12a
12d
12c
12b
OUTPUT CIRCUIT
12g
H×nbit
TO DISPLAY MEMORY 13

Fig. 3

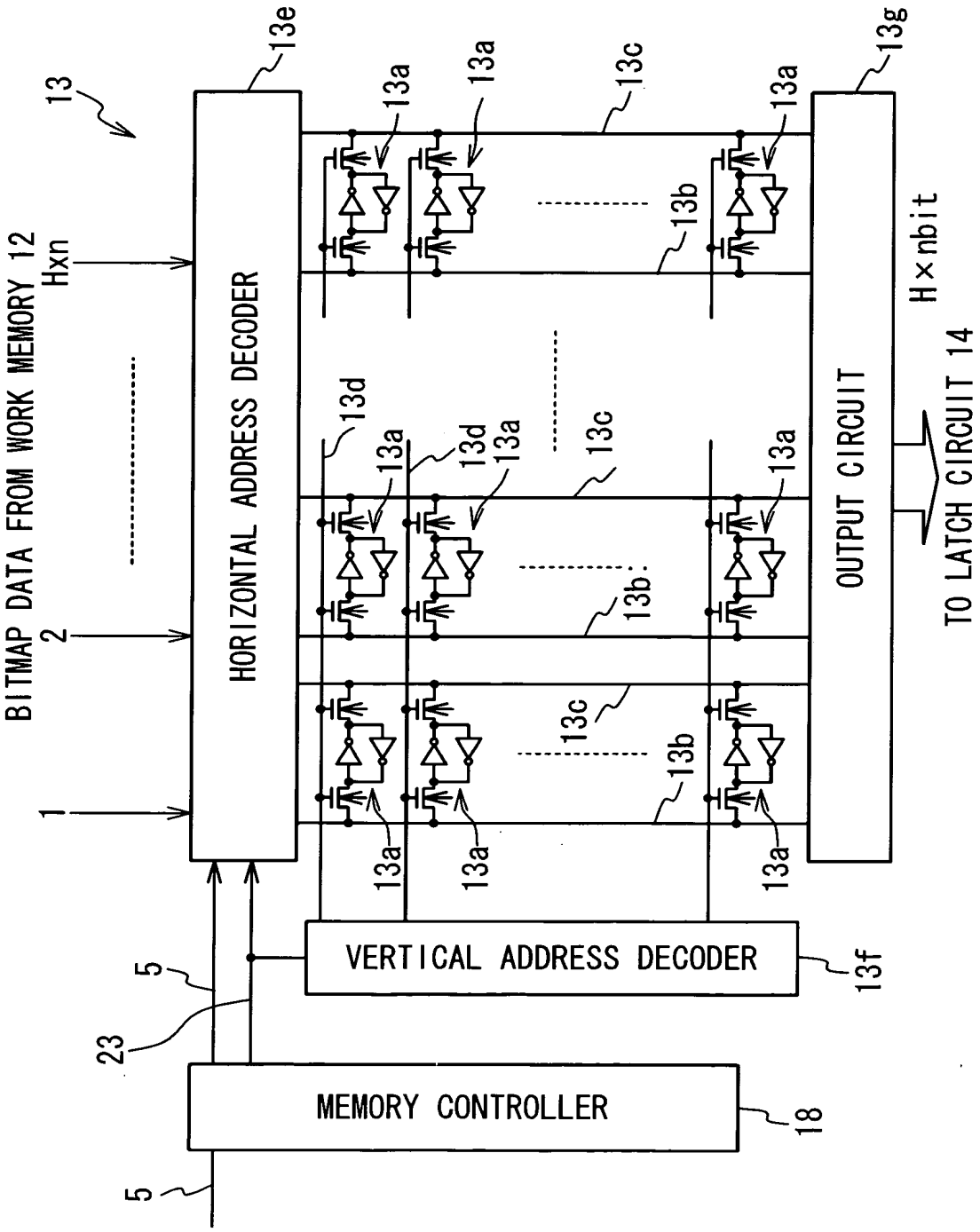

13
13e
13a
13a
13c
13a
13g
13b
BITMAP DATA FROM WORK MEMORY 12
Hxn
HORIZONTAL ADDRESS DECODER
OUTPUT CIRCUIT
H×nbit
TO LATCH CIRCUIT 14
13d
13d
13c
13b
2
1
VERTICAL ADDRESS DECODER
13f
5
23
MEMORY CONTROLLER
18
5

Fig. 4

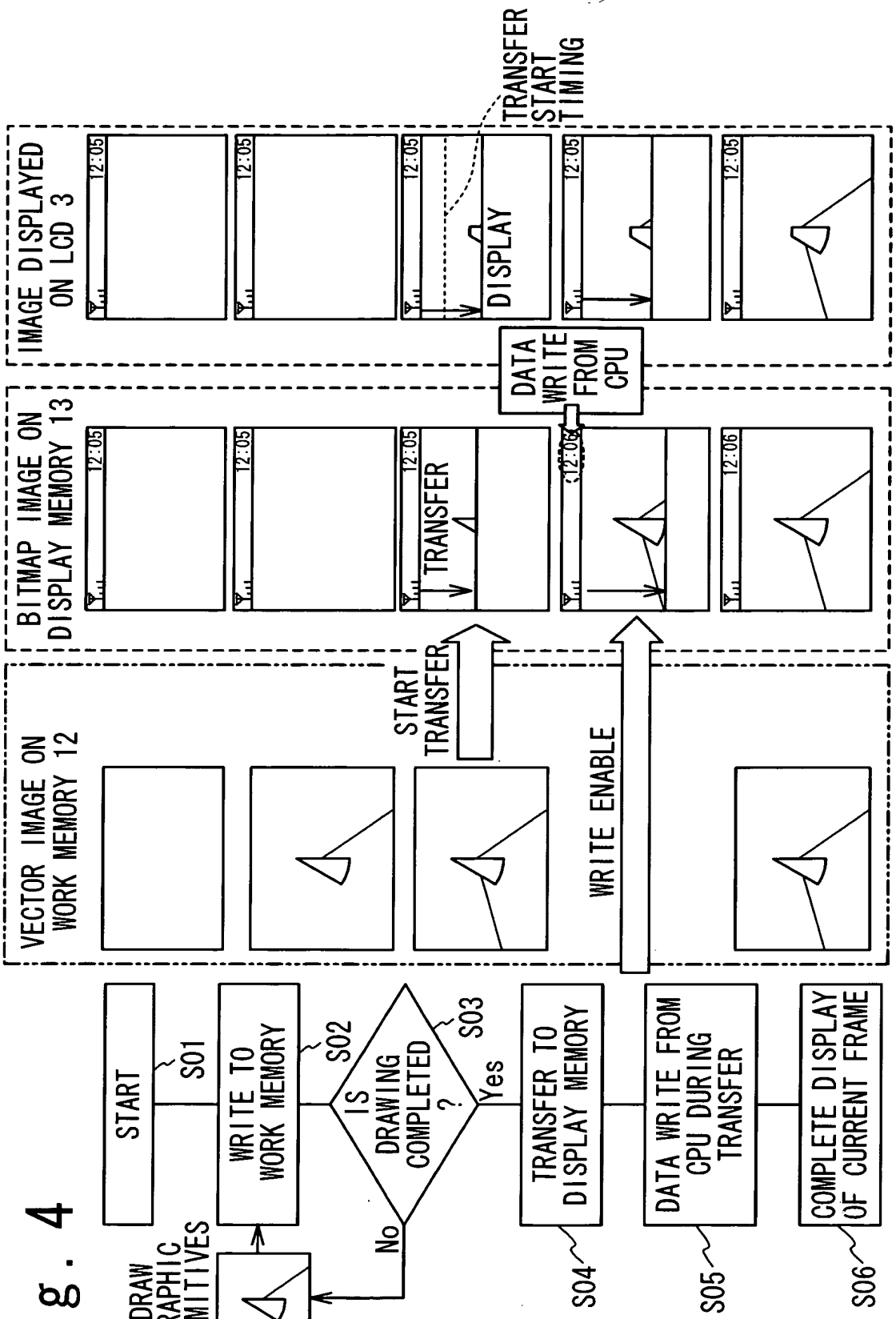

START
S01
WRITE TO WORK MEMORY
S02
IS DRAWING COMPLETED ?
S03
Yes
No
DRAW GRAPHIC PRIMITIVES
TRANSFER TO DISPLAY MEMORY
S04
DATA WRITE FROM CPU DURING TRANSFER
S05
COMPLETE DISPLAY OF CURRENT FRAME
S06
VECTOR IMAGE ON WORK MEMORY 12
START TRANSFER
WRITE ENABLE
BITMAP IMAGE ON DISPLAY MEMORY 13
TRANSFER
DATA WRITE FROM CPU
IMAGE DISPLAYED ON LCD 3
DISPLAY
TRANSFER START TIMING
12:05
12:06

Fig. 5

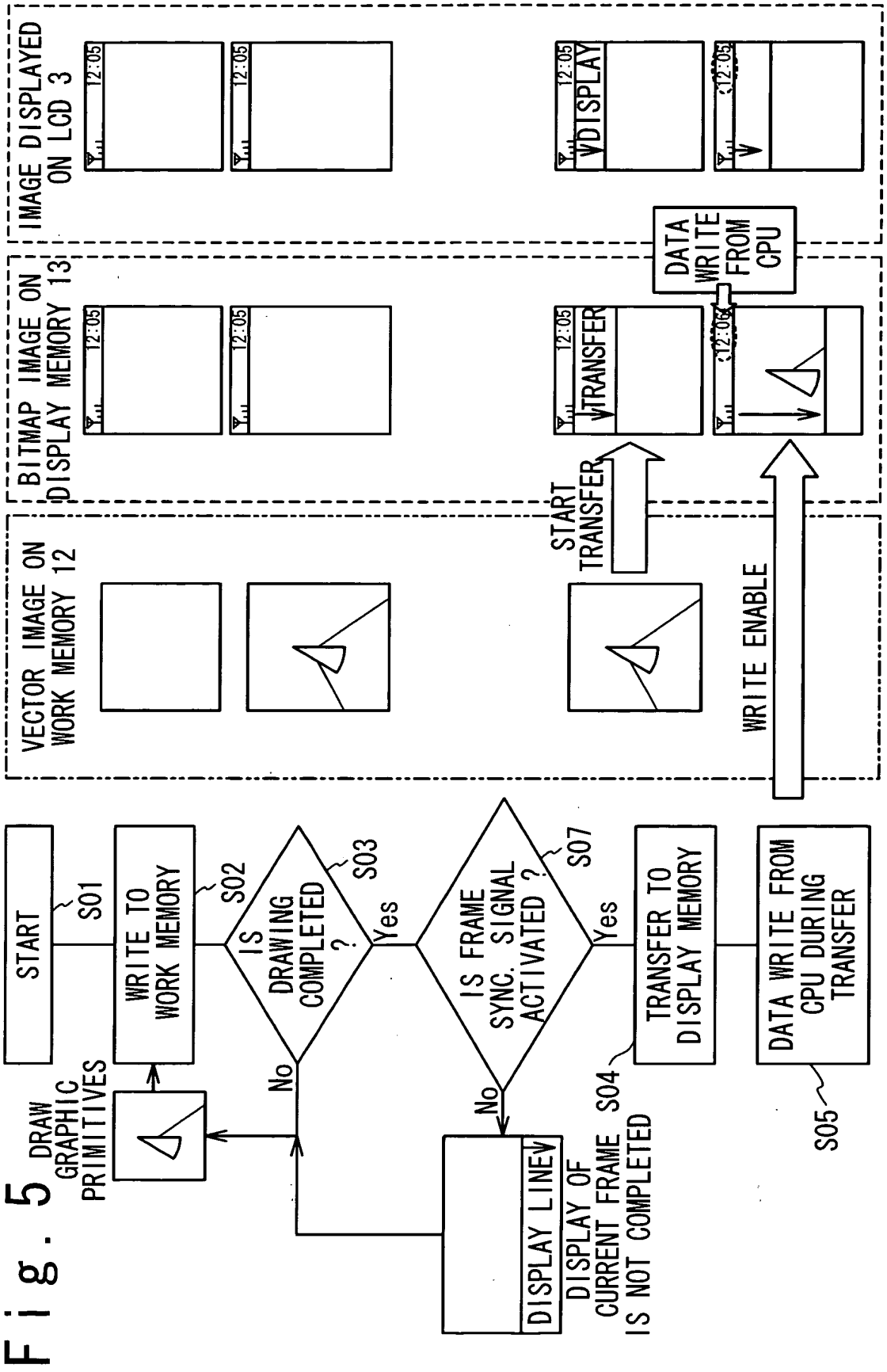
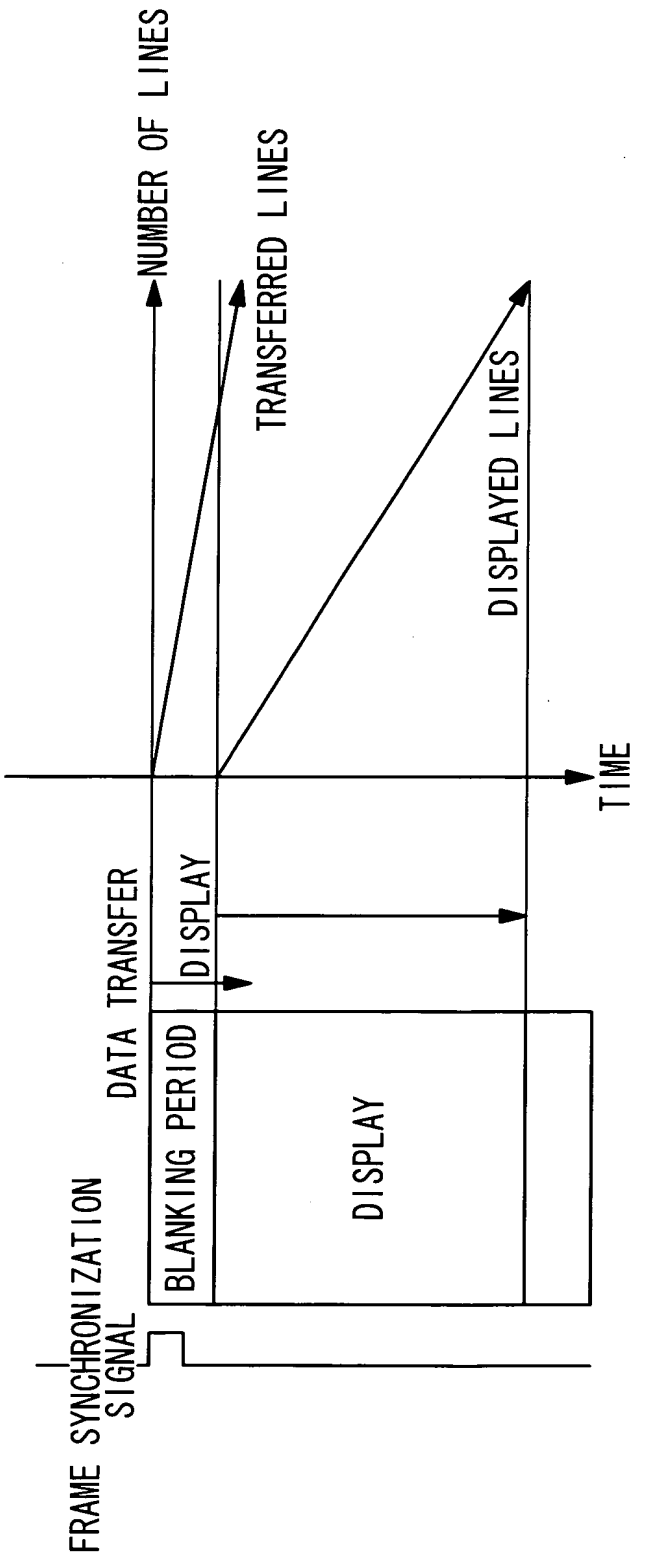


IMAGE DISPLAYED ON LCD 3
BITMAP IMAGE ON DISPLAY MEMORY 13
VECTOR IMAGE ON WORK MEMORY 12
DATA WRITE FROM CPU
START TRANSFER
WRITE ENABLE
START
S01
WRITE TO WORK MEMORY
S02
IS DRAWING COMPLETED ?
S03
Yes
No
IS FRAME SYNC. SIGNAL ACTIVATED ?
S07
Yes
No
TRANSFER TO DISPLAY MEMORY
S04
DATA WRITE FROM CPU DURING TRANSFER
S05
DRAW GRAPHIC PRIMITIVES
DISPLAY LINE
DISPLAY OF CURRENT FRAME IS NOT COMPLETED

Fig. 6


NUMBER OF LINES
TRANSFERRED LINES
DISPLAYED LINES
TIME
DATA TRANSFER
DISPLAY
BLANKING PERIOD
DISPLAY
FRAME SYNCHRONIZATION SIGNAL

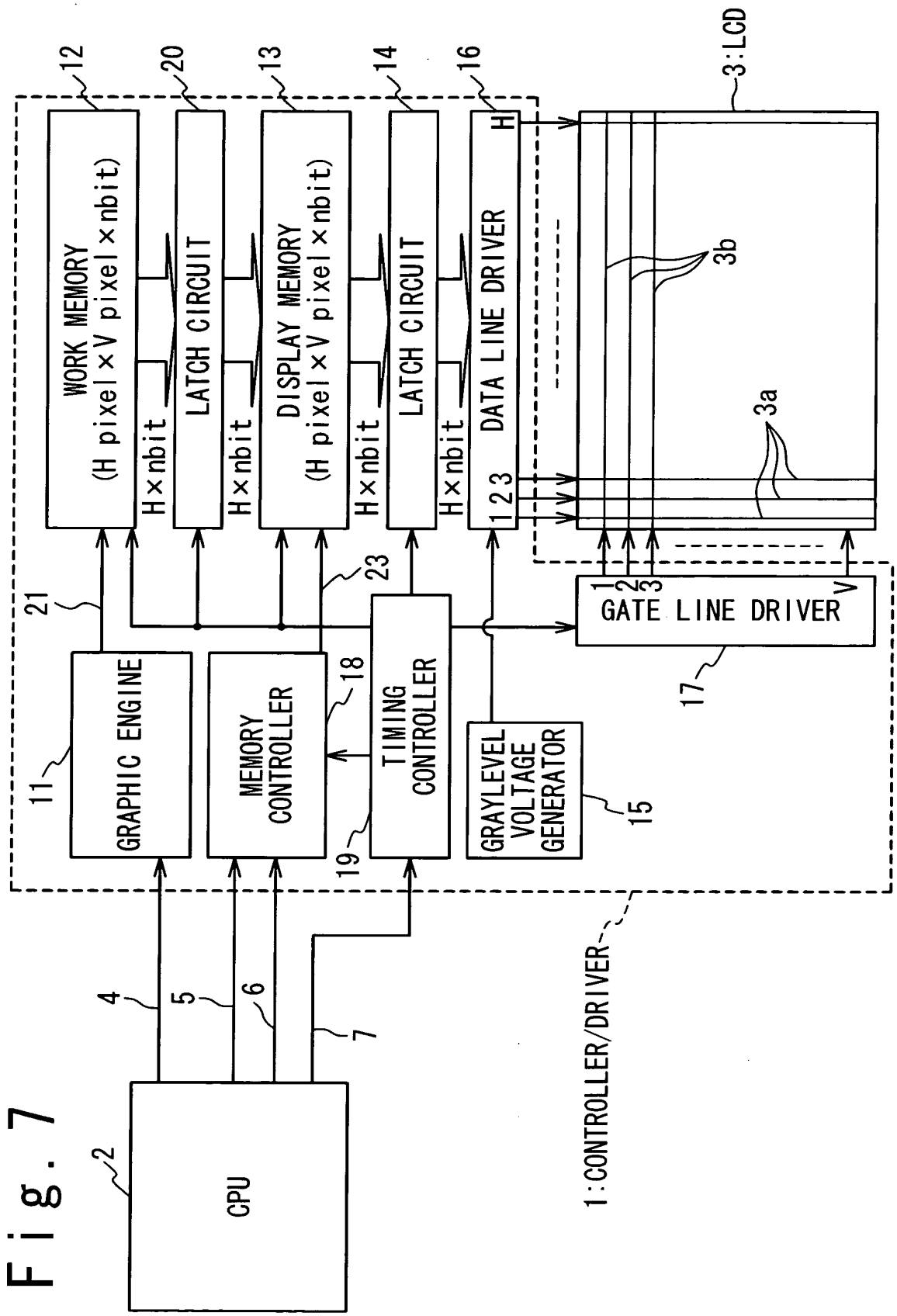

12
20
13
14
16
3:LCD
WORK MEMORY
(H pixel×V pixel×nbit)
LATCH CIRCUIT
DISPLAY MEMORY
(H pixel×V pixel×nbit)
LATCH CIRCUIT
DATA LINE DRIVER
H×nbit
H×nbit
H×nbit
H×nbit
H
1 2 3
V V V
3b
3a
21
23
GATE LINE DRIVER
1
2
3
V
17
11
GRAPHIC ENGINE
MEMORY CONTROLLER
18
TIMING CONTROLLER
19
GRAYLEVEL VOLTAGE GENERATOR
15
1:CONTROLLER/DRIVER
4
5
6
7
CPU
2

Fig. 7

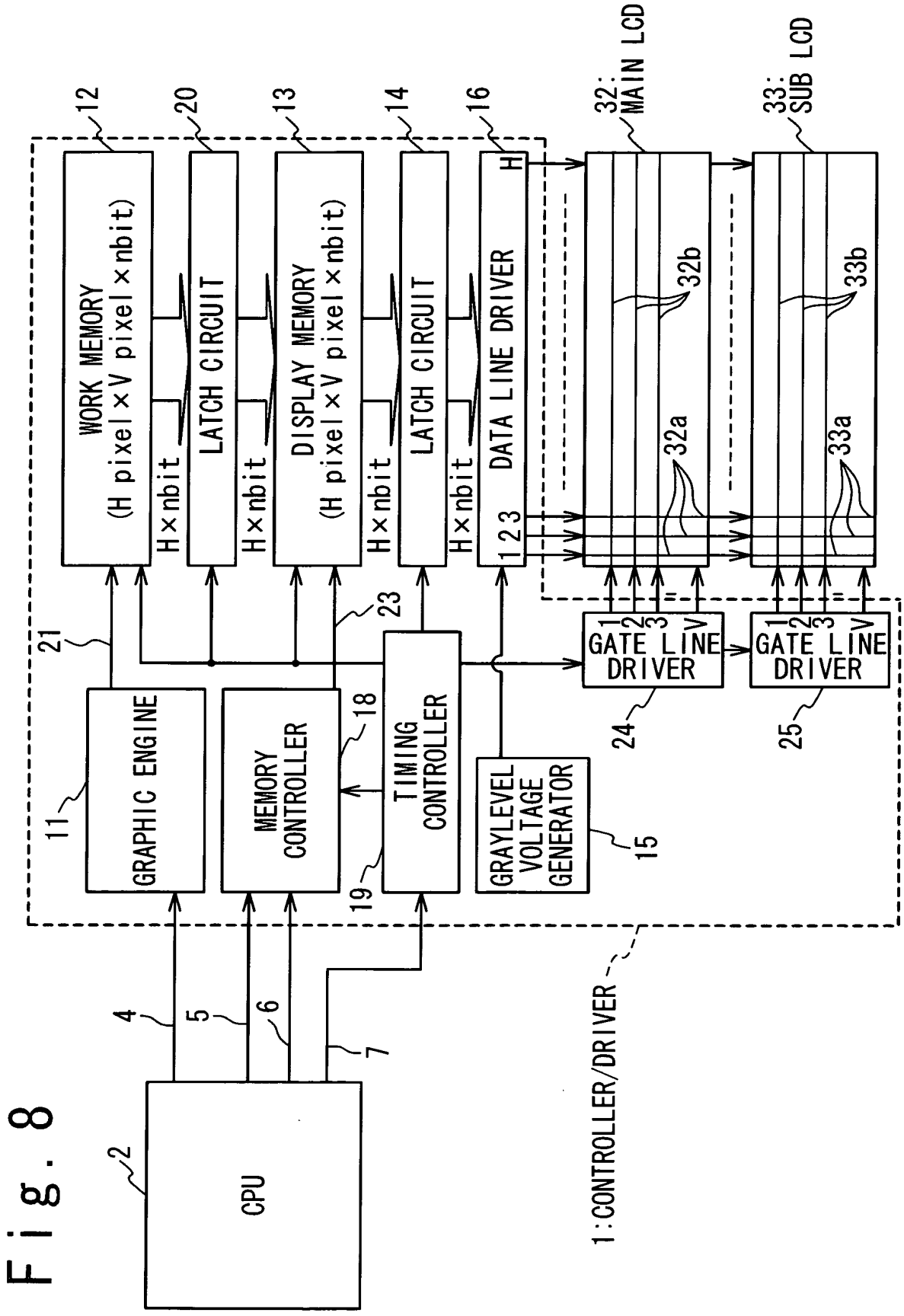

CPU
2
4
5
6
7
1:CONTROLLER/DRIVER
GRAPHIC ENGINE
11
MEMORY CONTROLLER
18
TIMING CONTROLLER
19
GRAYLEVEL VOLTAGE GENERATOR
15
21
23
GATE LINE DRIVER
24
GATE LINE DRIVER
25
1 2 3 V
WORK MEMORY (H pixel × V pixel × nbit)
12
LATCH CIRCUIT
20
DISPLAY MEMORY (H pixel × V pixel × nbit)
13
LATCH CIRCUIT
14
DATA LINE DRIVER
16
H
1 2 3
H × nbit
32: MAIN LCD
32a
32b
33: SUB LCD
33a
33b

Fig. 8

Fig. 9

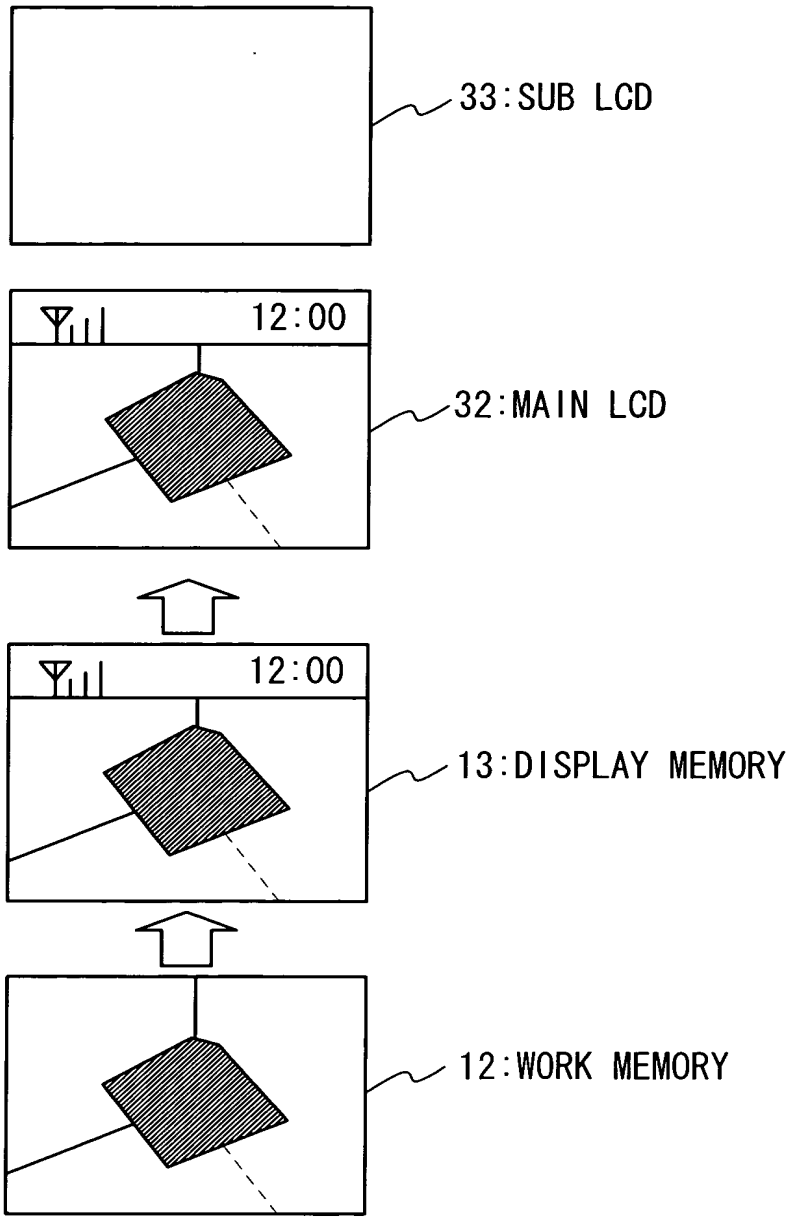

33:SUB LCD
12:00
32:MAIN LCD
12:00
13:DISPLAY MEMORY
12:WORK MEMORY

Fig. 10

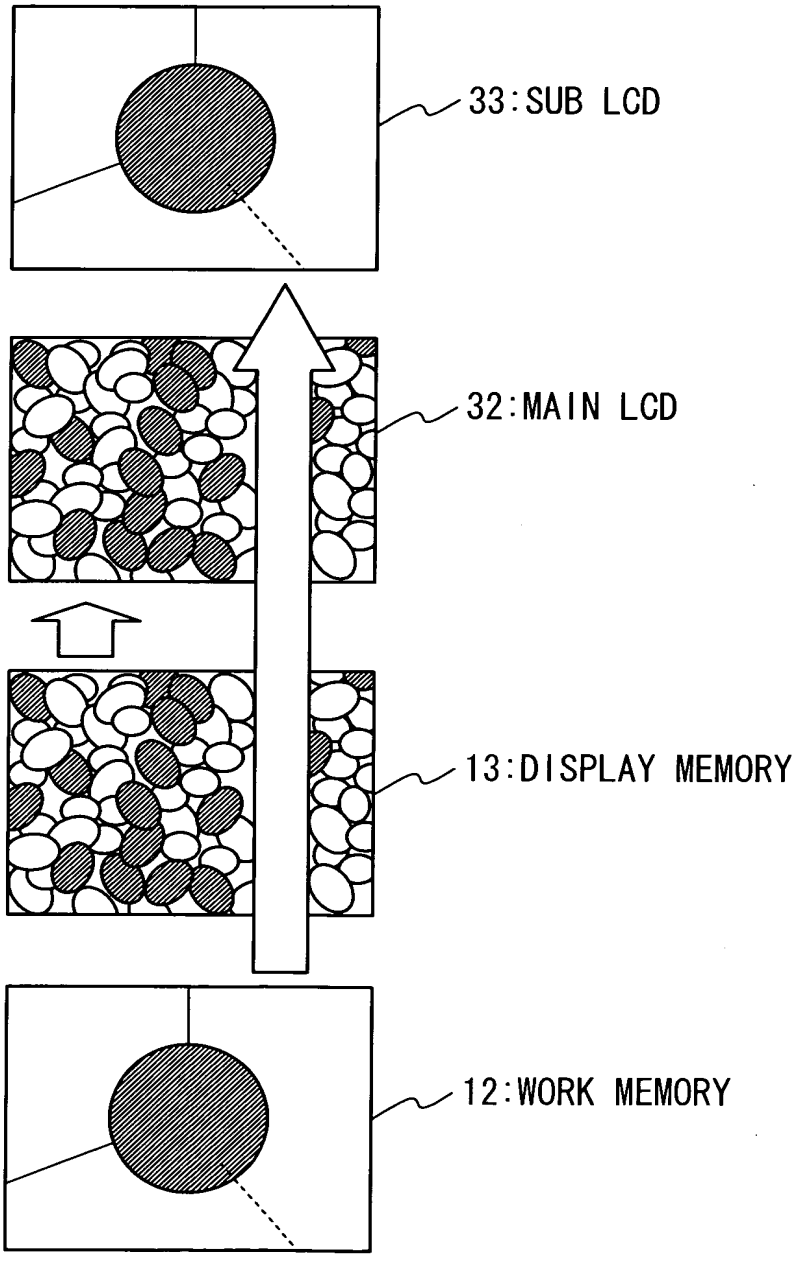


Fig. 11

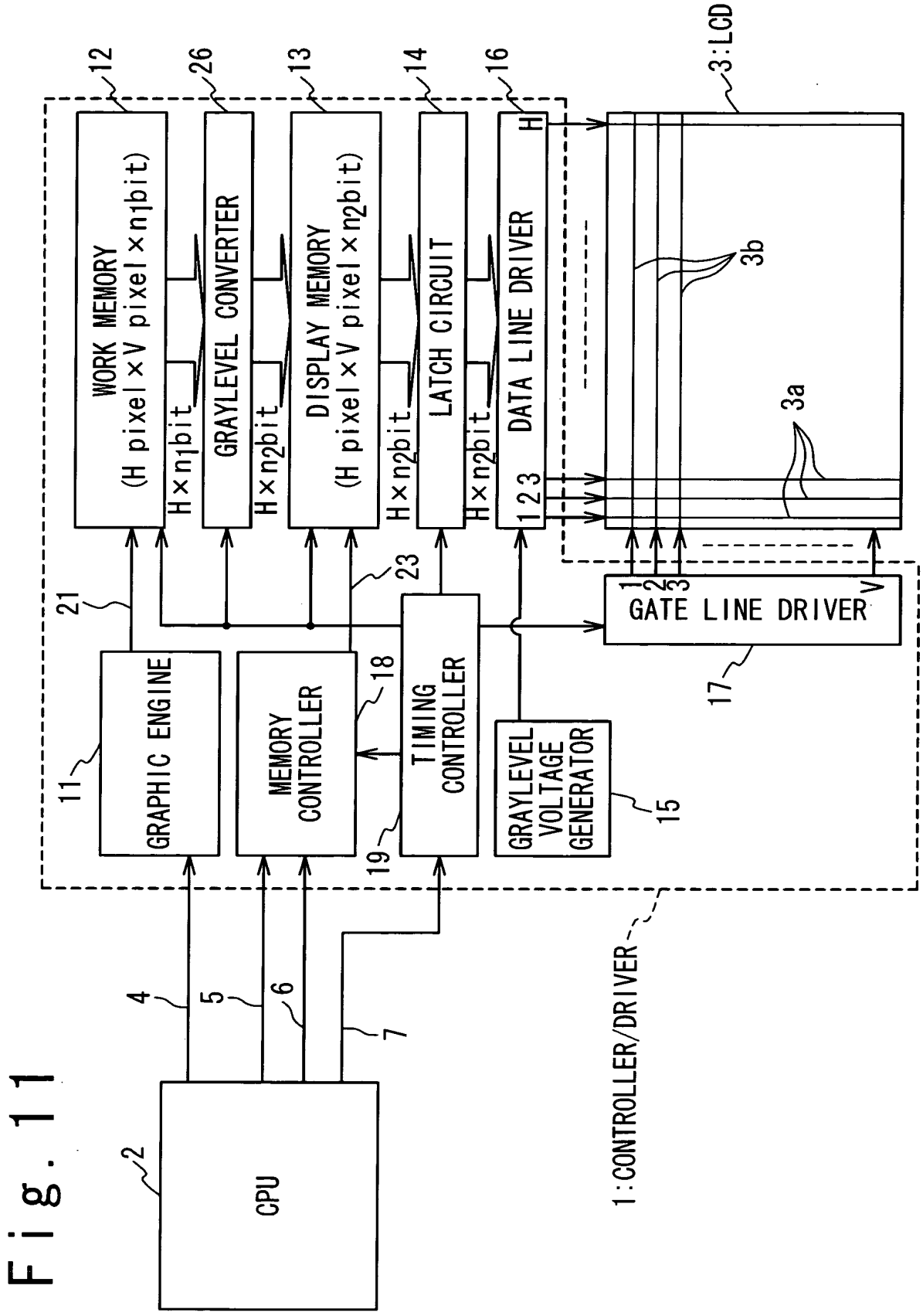
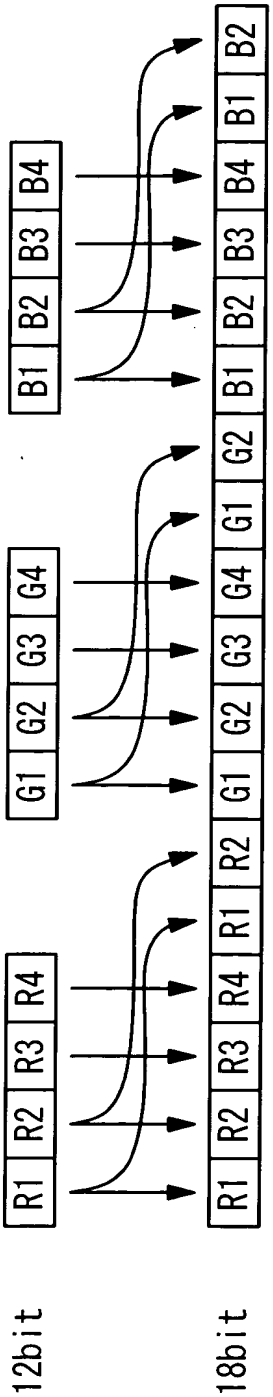

1:CONTROLLER/DRIVER
2
CPU
4
5
6
7
11
GRAPHIC ENGINE
12
WORK MEMORY
(H pixel × V pixel × n1bit)
H × n1bit
26
GRAYLEVEL CONVERTER
H × n2bit
13
DISPLAY MEMORY
(H pixel × V pixel × n2bit)
H × n2bit
14
LATCH CIRCUIT
H × n2bit
16
DATA LINE DRIVER
H
1 2 3
3:LCD
3b
3a
21
23
18
MEMORY CONTROLLER
19
TIMING CONTROLLER
GRAYLEVEL VOLTAGE GENERATOR
15
1 2 3 V
GATE LINE DRIVER
17

Fig. 12


R1 R2 R3 R4
G1 G2 G3 G4
B1 B2 B3 B4
12bit
R1 R2 R3 R4 R1 R2 G1 G2 G3 G4 G1 G2 B1 B2 B3 B4 B1 B2
18bit

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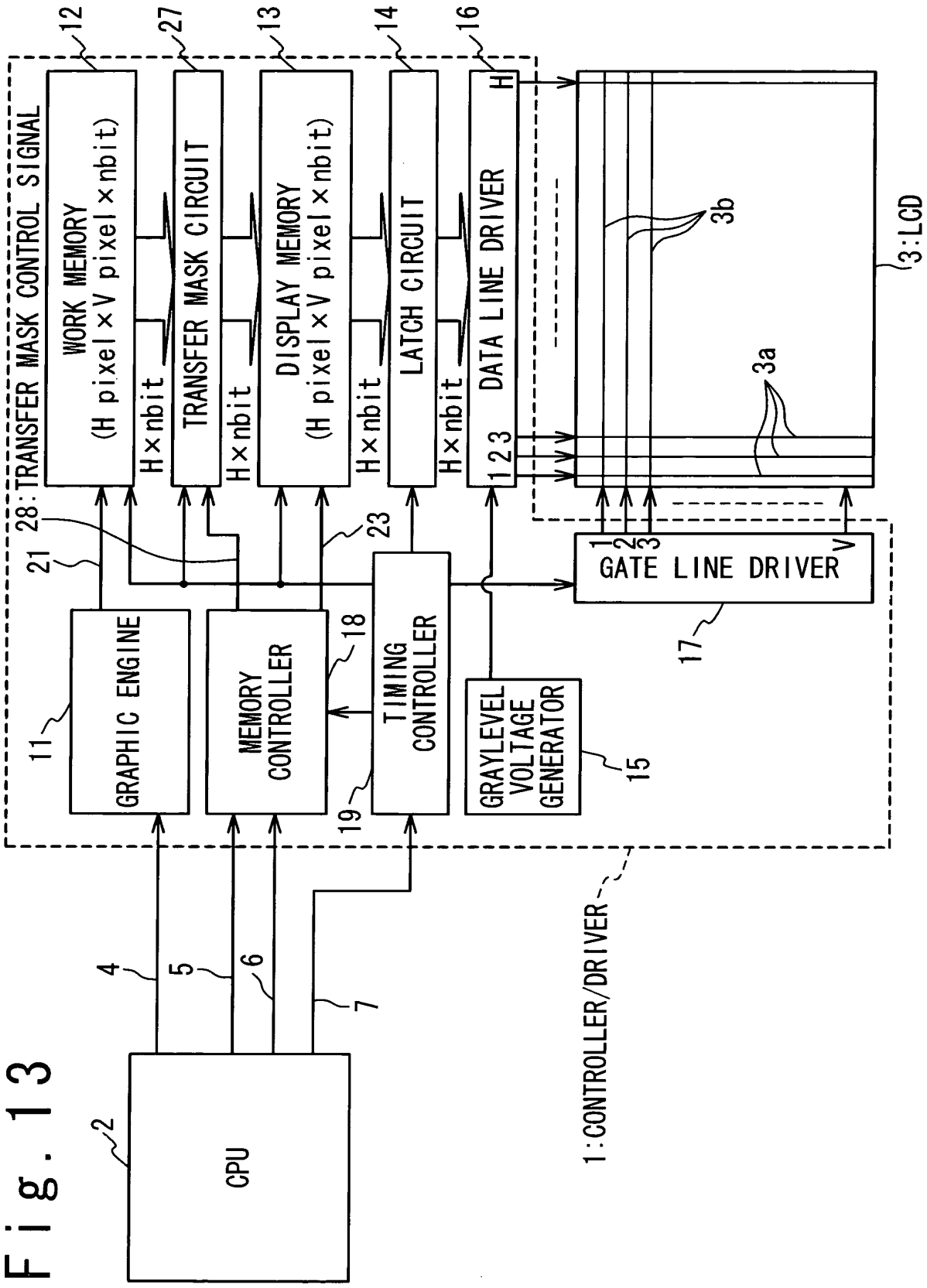


Fig. 13

Fig. 14

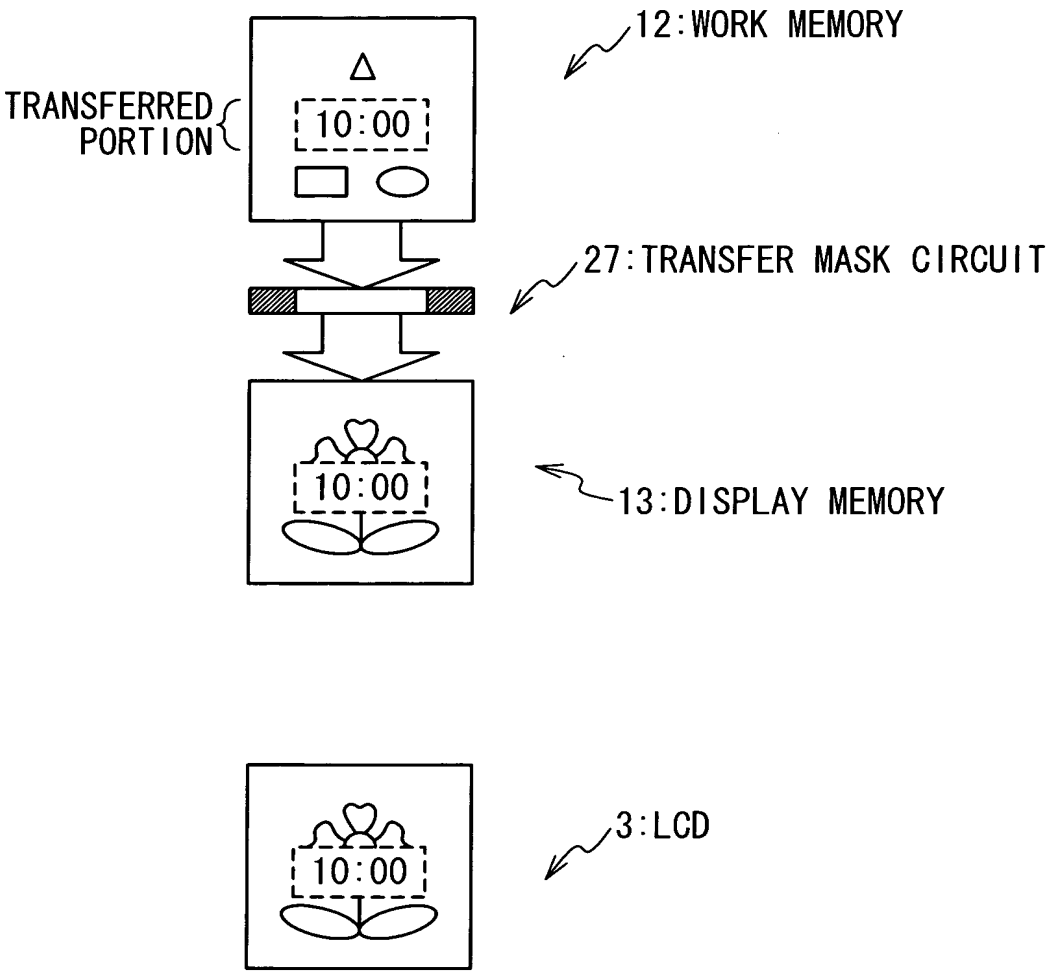

12:WORK MEMORY
TRANSFERRED PORTION
10:00
27:TRANSFER MASK CIRCUIT
10:00
13:DISPLAY MEMORY
10:00
3:LCD

Fig. 15

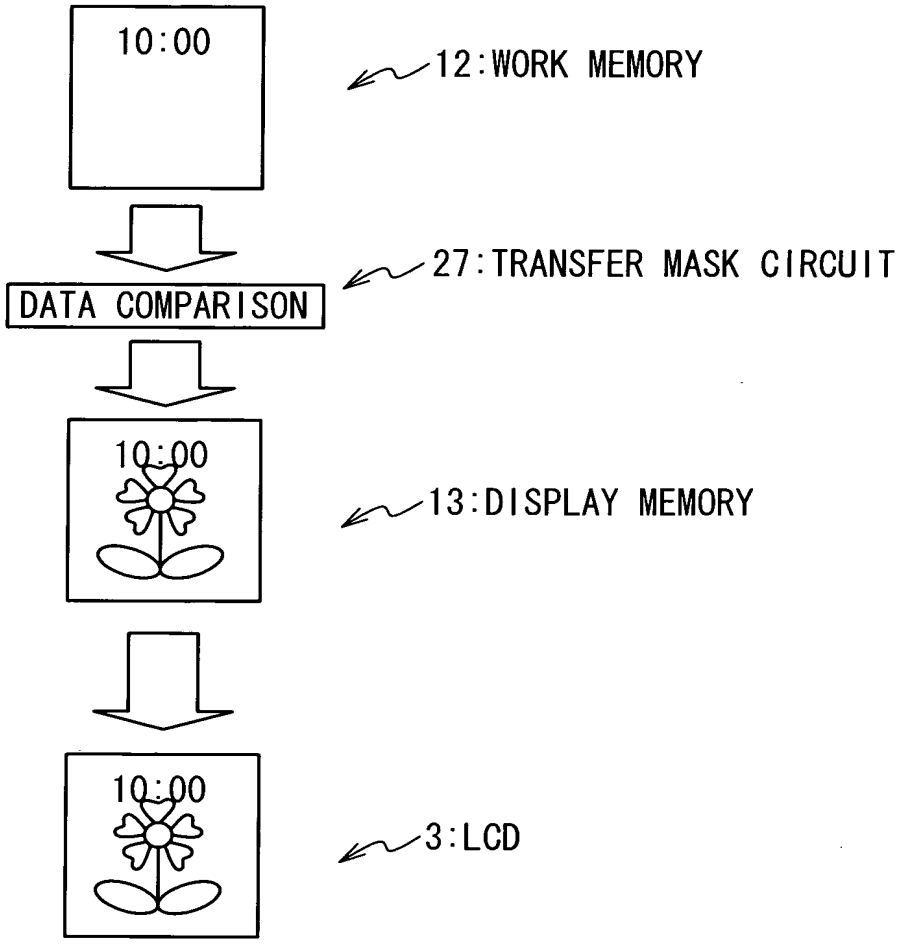

10:00
12:WORK MEMORY
DATA COMPARISON
27:TRANSFER MASK CIRCUIT
10:00
13:DISPLAY MEMORY
10:00
3:LCD

Fig. 16

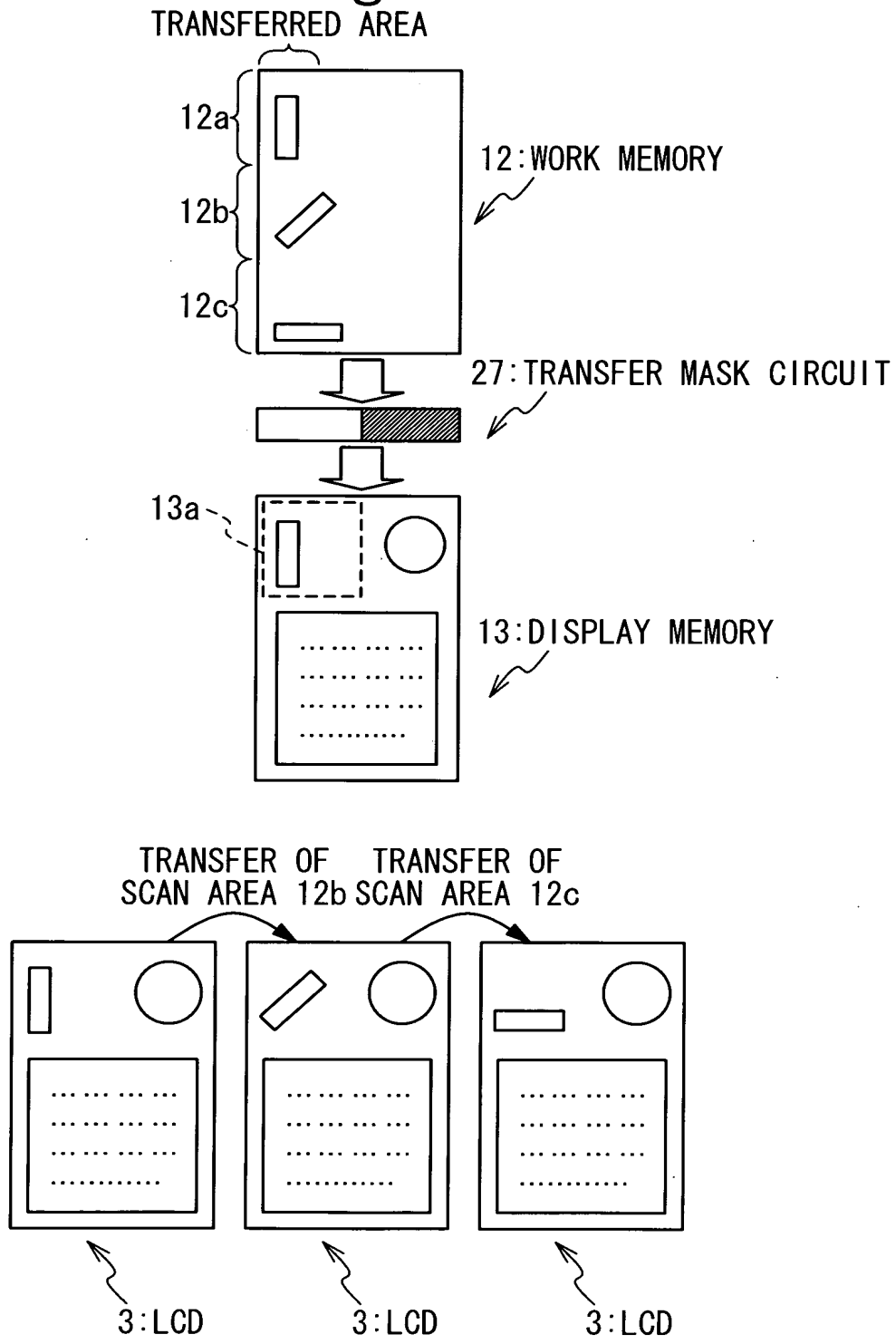

TRANSFERRED AREA
12a
12b
12c
12:WORK MEMORY
27:TRANSFER MASK CIRCUIT
13a
13:DISPLAY MEMORY
TRANSFER OF SCAN AREA 12b
TRANSFER OF SCAN AREA 12c
3:LCD
3:LCD
3:LCD

Fig. 17

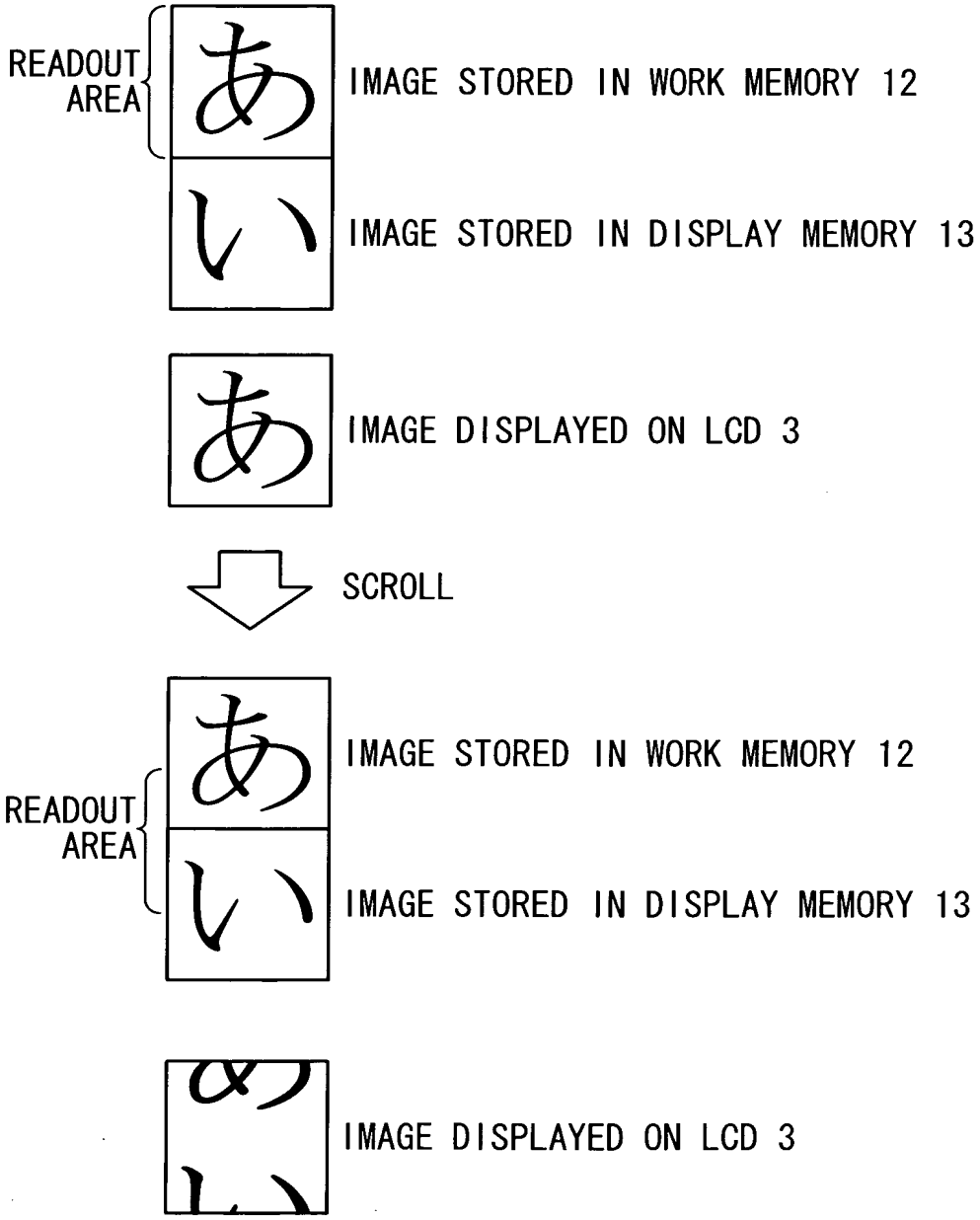
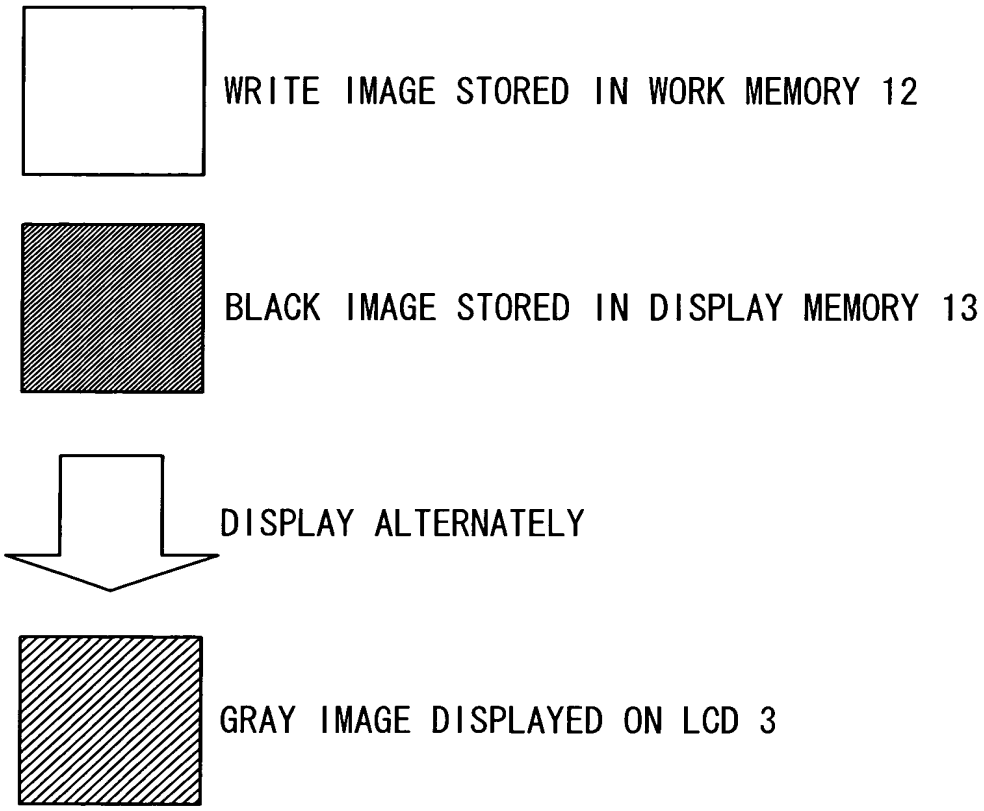

READOUT AREA
あ
IMAGE STORED IN WORK MEMORY 12
い
IMAGE STORED IN DISPLAY MEMORY 13
あ
IMAGE DISPLAYED ON LCD 3
SCROLL
READOUT AREA
あ
IMAGE STORED IN WORK MEMORY 12
い
IMAGE STORED IN DISPLAY MEMORY 13
IMAGE DISPLAYED ON LCD 3

Fig. 18


WRITE IMAGE STORED IN WORK MEMORY 12
BLACK IMAGE STORED IN DISPLAY MEMORY 13
DISPLAY ALTERNATELY
GRAY IMAGE DISPLAYED ON LCD 3

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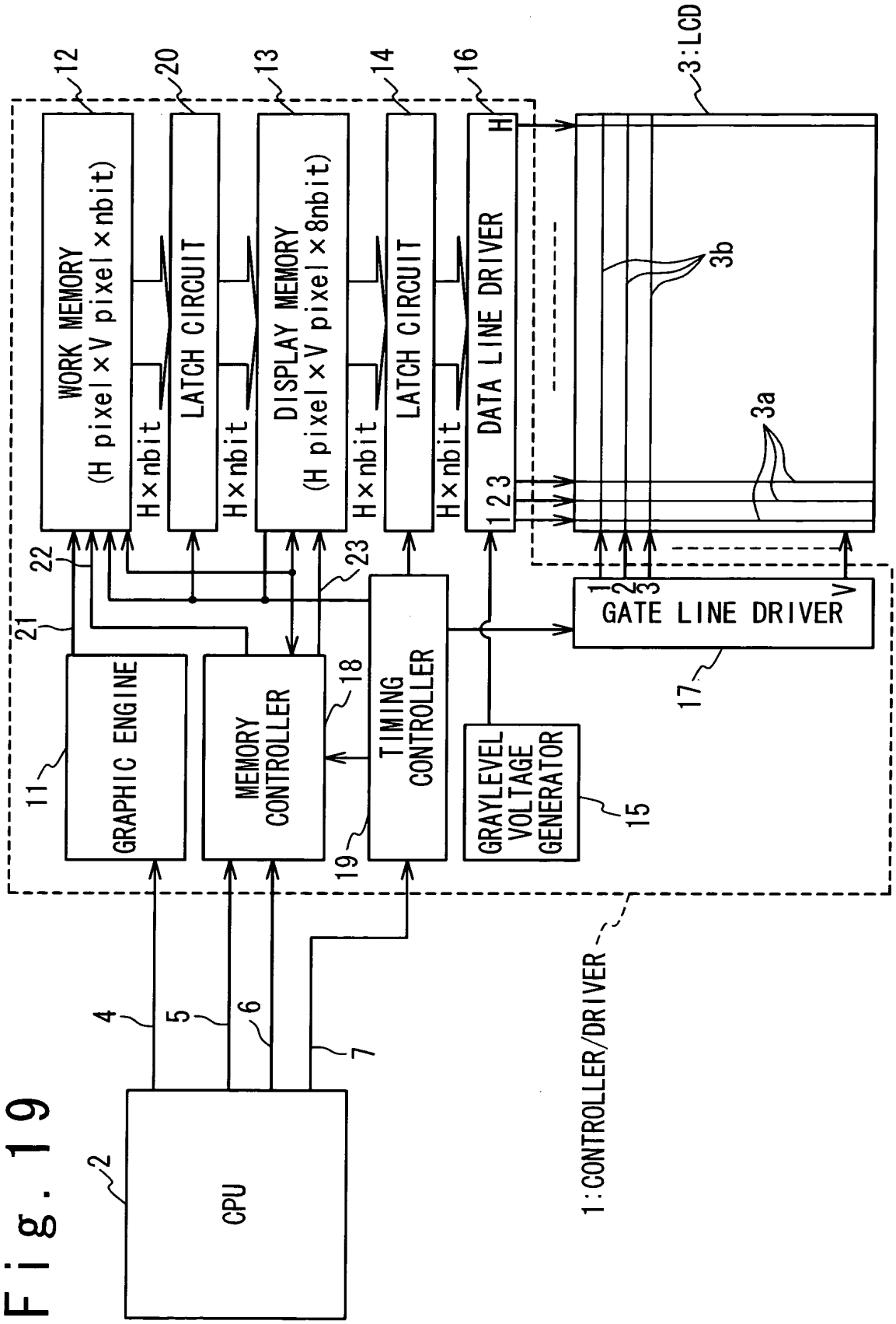


Fig. 19

Fig. 20

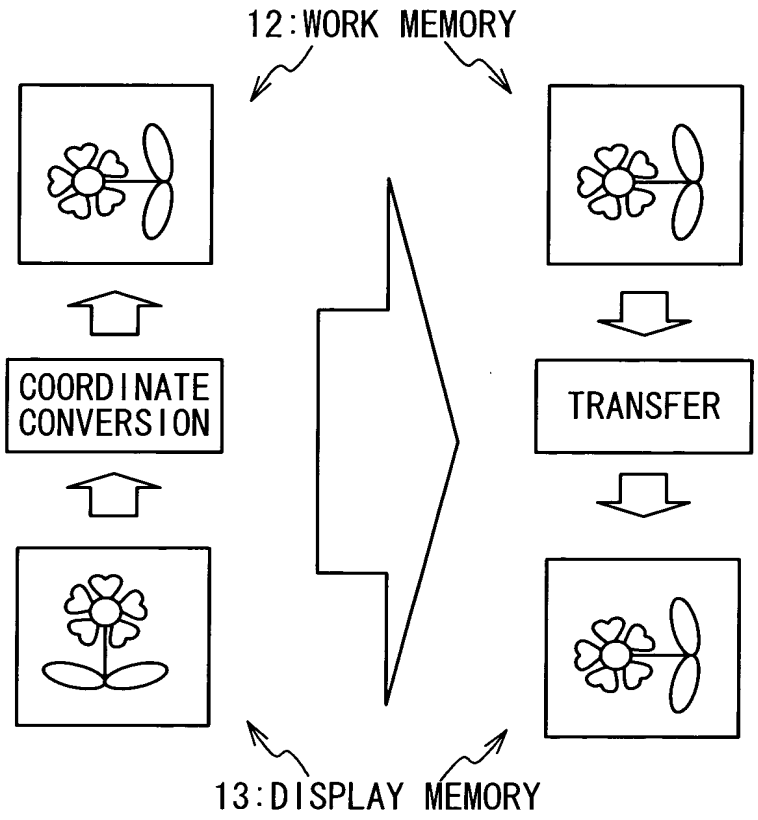

12:WORK MEMORY
COORDINATE CONVERSION
TRANSFER
13:DISPLAY MEMORY

Fig. 21

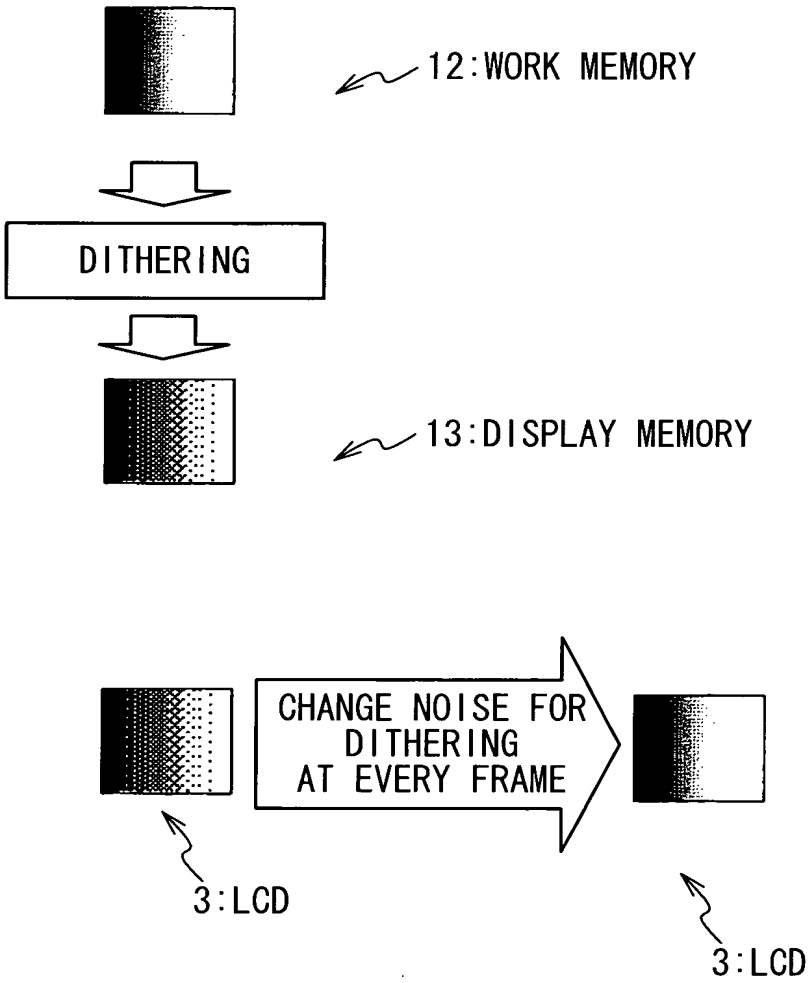

12:WORK MEMORY
DITHERING
13:DISPLAY MEMORY
CHANGE NOISE FOR
DITHERING
AT EVERY FRAME
3:LCD
3:LCD

Fig. 22A

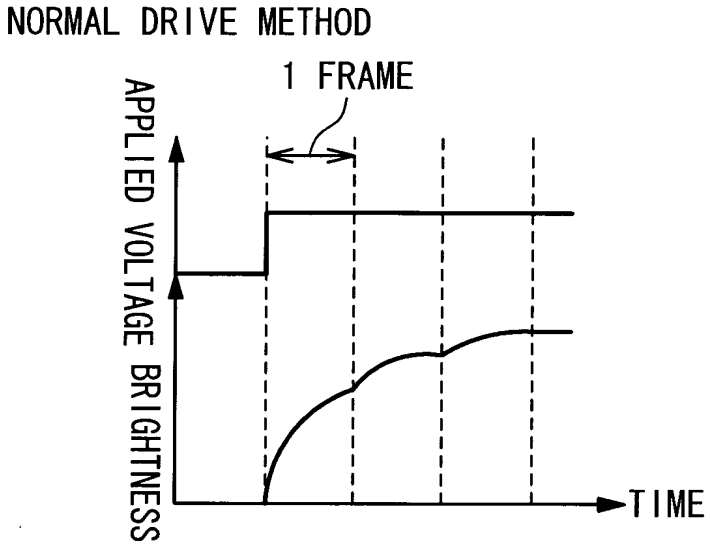


Fig. 22B

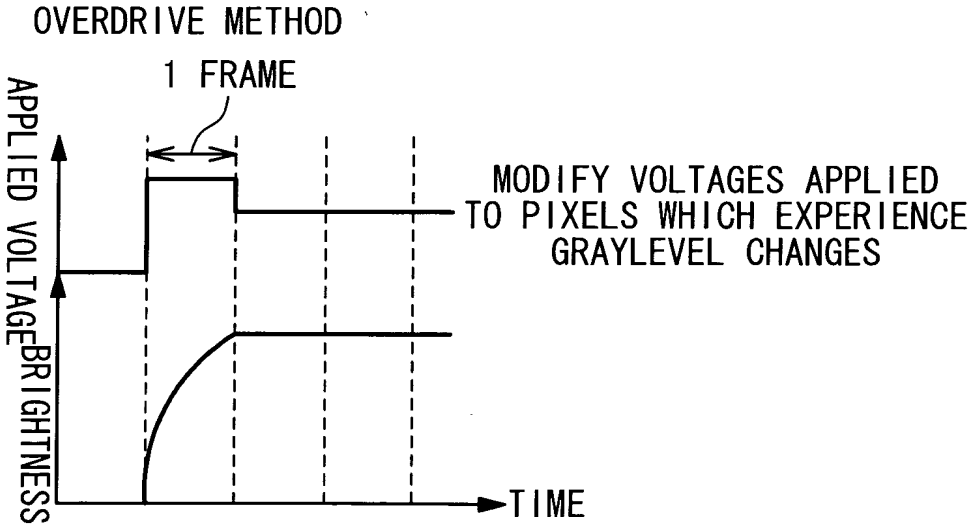


Fig. 23A

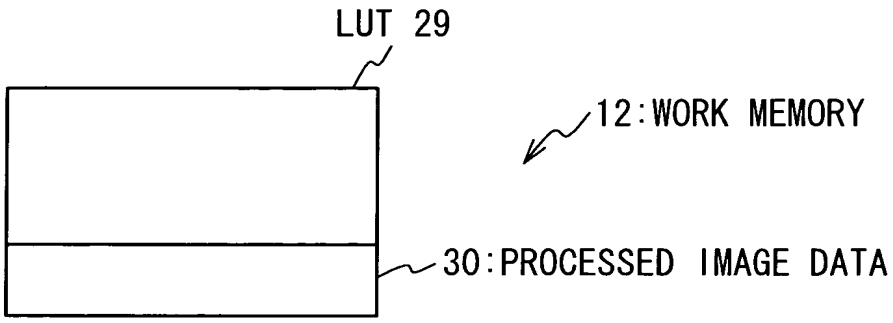
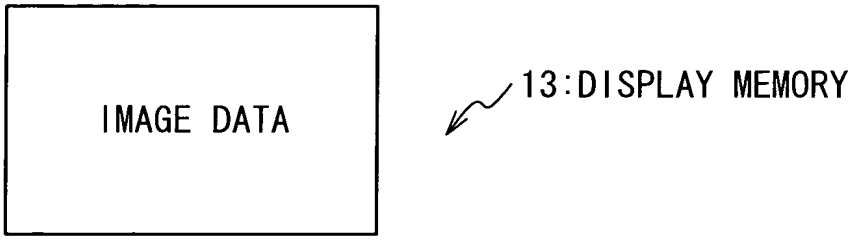


Fig. 23B



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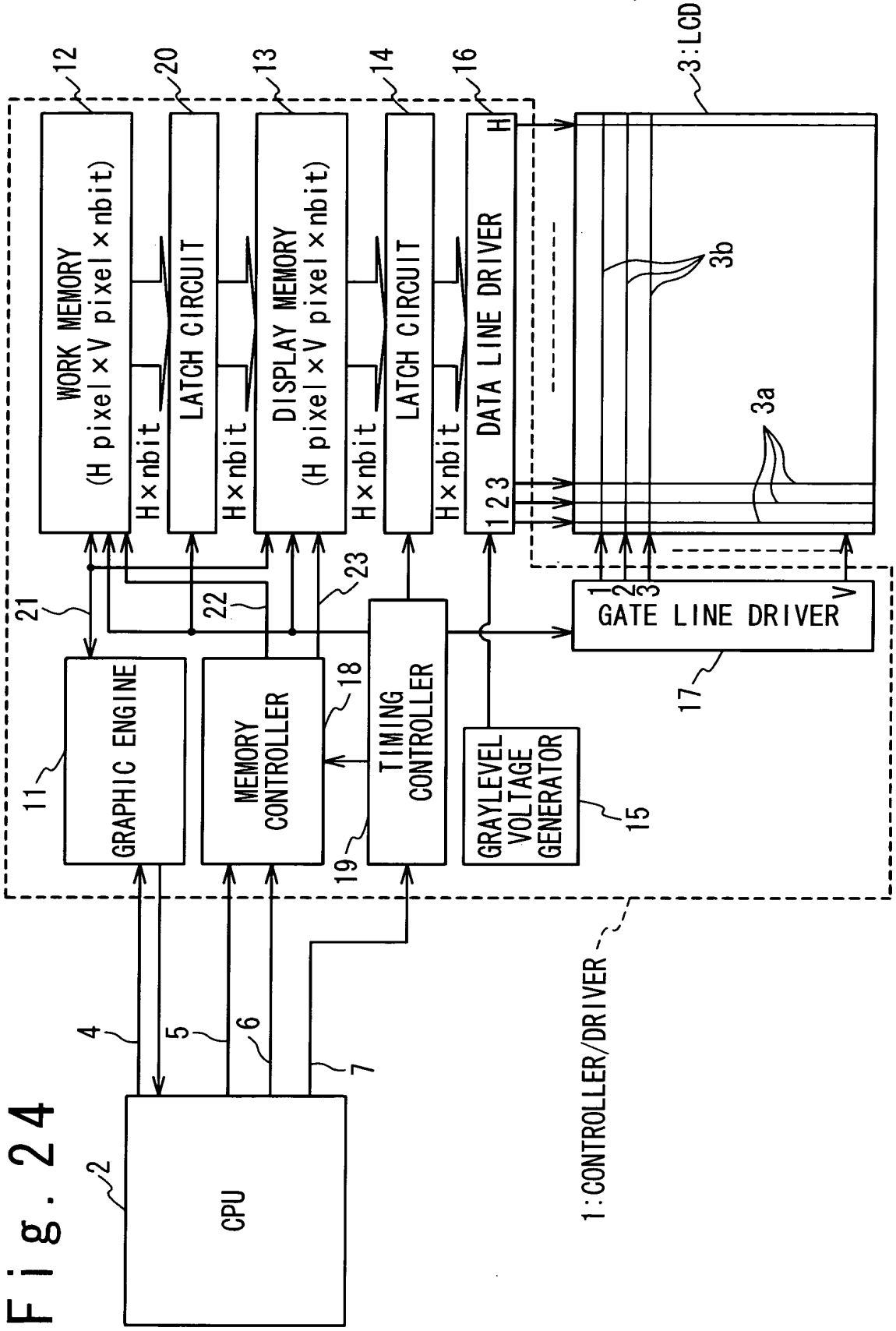

Fig. 24

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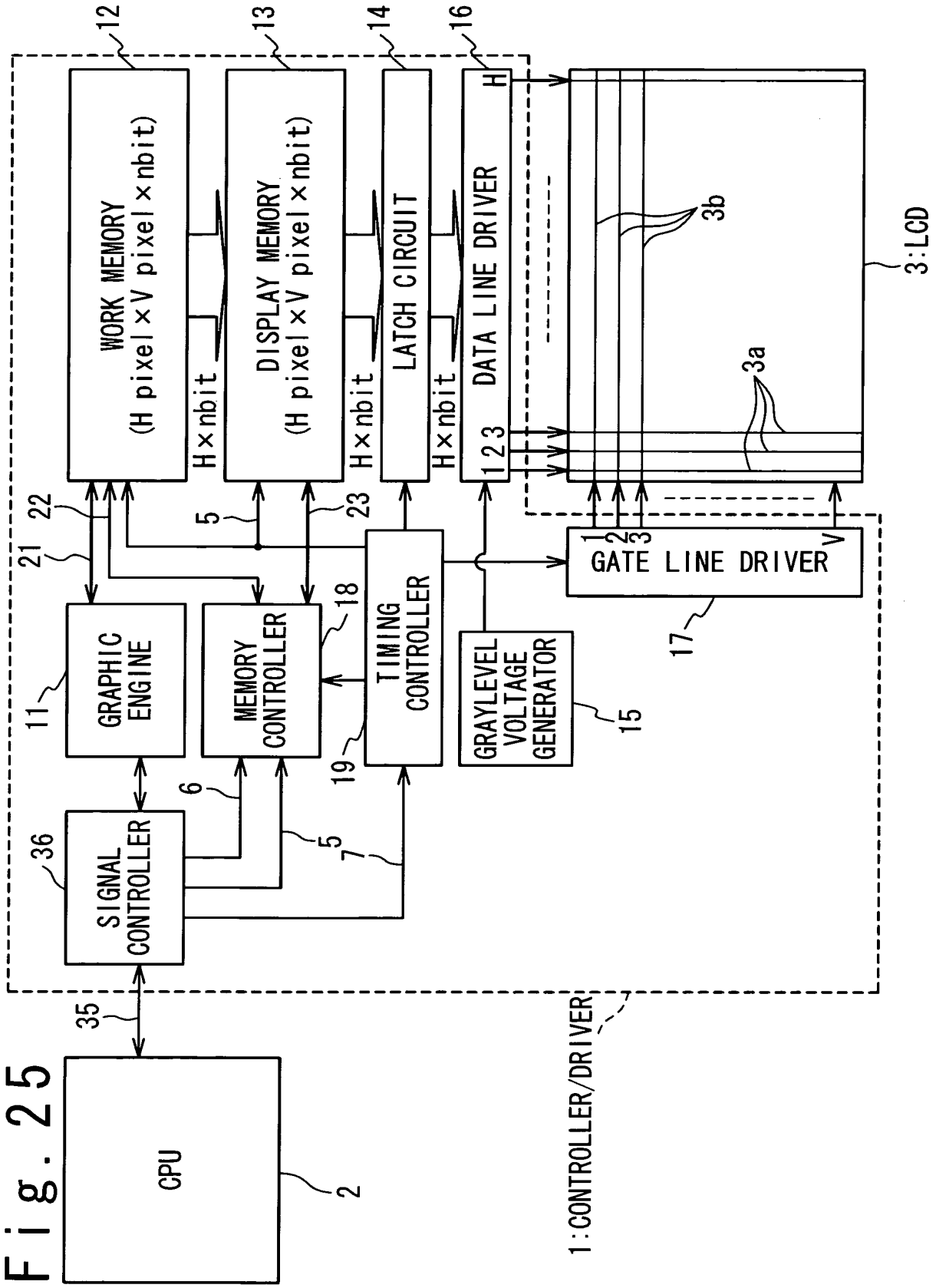

Fig. 25